First Demonstration of BEOL-Compatible Atomic-Layer-Deposited InGaZnO TFTs with 1.5 nm Channel Thickness and 60 nm Channel Length Achieving ON/OFF Ratio Exceeding 10^{11}, SS of 68 mV/dec, Normal-off Operation and High Positive Gate Bias Stability

Jie Zhang[1], Zhuocheng Zhang[1], Zehao Lin[1], Ke Xu[2], Hongyi Dou[2], Bo Yang[2], Xinghang Zhang[2], Haiyan Wang[2] and Peide D. Ye[1*]
[1]Elmore Family School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47907, U.S.A. *Email: yep@purdue.edu
[2]School of Materials Engineering , Purdue University, West Lafayette, IN, U.S.A.

Abstract

In this work, we report on the first demonstration of atomic-layer-deposited (ALD) InGaZnO (IGZO) thin film transistors (TFTs) with extreme scaled channel thickness (T_{ch}) of 1.5 nm and channel length (L_{ch}) of 60 nm. These ALD IGZO TFTs exhibit desirable electrical performance including a high on/off ratio exceeding 10^{11}, a steep subthreshold swing (SS) of 68 mV/dec, a small DIBL of 30 mV/V and a normal-off operation. By optimizing the duration of O_2 annealing at 250 °C, the threshold voltage (V_T) roll-off issue at scaled L_{ch} is resolved together with a remarkably high degree of stability to the positive gate bias stress (PBS). A trap model with its possible microscopic origin is proposed, providing a new insight into the reliability of IGZO TFTs.

Introduction

Recent work on scaled IGZO TFTs have extended their application domain from the traditional back-plane display to BEOL-compatible logic and memory applications towards monolithic 3D integration [1-6]. These scaled IGZO TFTs were derived by sputtering method, exhibiting excellent performance with high I_{on} and thus revitalizing the prospects of IGZO as a TFT channel material. Compared to sputtering, ALD growth method provides more precise thickness control, excellent conformity, composition flexibility and large-area uniformity, benefiting to the realization of the ultra-scaled TFTs. However, to the best of our knowledge, scaled ALD IGZO TFTs are still missing. Furthermore, previous scaled sputtered IGZO TFTs show a V_T roll-off issue [1-5], leading to a normal-on operation for the ultra-scaled TFTs. Additionally, the gate bias stability was also not evaluated in these reports [1-6], which is essential for the practical applications.

In this work, we report for the first time ALD IGZO TFTs with extreme scaled T_{ch} of 1.5 nm and L_{ch} of 60 nm, exhibiting outstanding electrical performance including a high I_{on}/I_{off} exceeding 10^{11}, a steep SS of 68 mV/dec, a high I_{on} of 354 μA/μm at V_{DS} of 1.2 V, a small DIBL of 30 mV/V and a normal-off operation. The threshold V_T roll-off issue at scaled L_{ch} is significantly alleviated by longer O_2 annealing time. Furthermore, a remarkably high degree of stability to PBS is achieved via optimizing O_2 annealing. A trap model with its possible microscopic origin is proposed, offering guidance for future device optimization. The key highlights of this work are shown in Fig.1.

Experiments

Figure 2(a) illustrates the schematic of an ultrathin IGZO TFT with the T_{ch} ranging from 0.7 nm to 4.3 nm, where 40 nm Ni, 6 nm HfO_2 function as electrode and dielectric, respectively. The IGZO channel was deposited by ALD at 225 °C, with one cycle of ZnO and Ga_2O_3 followed by 10 cycles of In_2O_3 forming one super-cycle of the IGZO growth. The IGZO channel thickness was controlled by the number of super-cycles with a growth rate of ~1.25 Å/super-cycle, which was examined by an ellipsometer and HRTEM. The detailed TFT fabrication process is depicted in Fig.2(b). After device fabrication, these TFTs were subjected to O_2 annealing at 250 °C for 1min, 10 min and 30 min, respectively. The HRTEM image of an ultrascaled IGZO TFT with T_{ch} of 1.5 nm and L_{ch} of 60 nm is shown in Fig.2(c). The chemical composition of the 1.5nm ALD IGZO film was analyzed by XPS (Fig.3), exhibiting a high In ratio of ~92%/4%/4% for In/Ga/Zn, respectively, which is beneficial for achieving high I_{on} for IGZO TFTs.

Results and Discussion

Figure 4 (a) illustrates bi-directional transfer characteristics of IGZO TFTs with a L_{ch} of 60 nm and various T_{ch} of 0.7 nm to 4.3 nm under V_{DS} of 0.5 V using optimized 10 min O_2 annealing. It is found that the T_{ch} has a significant effect on the electron transport in the IGZO channel. The IGZO TFTs with T_{ch} of 0.7 nm show no observable current while that of 1.5 nm to 4.3 nm exhibit a well-behaved performance. This is in contrast to that pure In_2O_3 TFTs with T_{ch} of 0.7 nm could still be operational [7], suggesting that Zn and Ga could function as carrier suppressors and transport hinders in the In_2O_3 host. The V_T is also found to be negatively shifted accompanied with an enhanced current drivability as T_{ch} is increased from 1.5 nm to 4.3 nm, which is expected due to the increased two-dimensional electron density in the IGZO channel. Only TFTs with T_{ch} of 1.5 nm exhibit a normal-off operation, which is determined by a linear extrapolation method and highly desirable for BEOL applications. Note that all TFTs show a negligible hysteresis, suggesting a high-quality channel/dielectric interface, which is also evidenced by the nearly ideal SS of ~68 mV/dec. Figure 4(b) exhibits transfer curves of TFTs with T_{ch} of 1.5 nm and L_{ch} of 60 nm under varying V_{DS} from 0.05 V to 1.2 V. A high I_{on}/I_{off} of $>10^{11}$ and a small DIBL of ~30 mV/V can be observed. The maximum g_m for TFTs with L_{ch} of 60 nm and varying T_{ch} can be found in Fig.4(c). Our ALD IGZO TFTs show a high g_m value of ~151 μS/μm to 265 μS/μm, which are among the best values for the IGZO TFTs. Note that the maximum applied V_{DS} before severe self-heating occurring [8] is increased with the reduced T_{ch} and less I_{on} thus less generated heat. Figure 5(a) shows the output characteristics of IGZO TFTs with L_{ch} of 60 nm and T_{ch} of 1.5 nm, where a relatively high I_{on} of 354 μA/μm can be observed under V_{DS} of 1.2 V. An extreme high I_{on} of 1080 μA/μm can be achieved in Fig.5(b) for TFTs with T_{ch} of 4.3 nm under V_{DS} of 0.8 V.

Such excellent performance could be attributed to the combinatorial effects of ultrathin channel and optimized O_2 annealing. Figures 6(a)-(c) illustrates bi-directional transfer characteristics of IGZO TFTs with T_{ch} of 1.5 nm and L_{ch} ranging from 1 μm to 60 nm under V_{DS} of 0.5 V, which have undergone O_2 annealing for 1 min, 10 min and 30 min, respectively. A shrinking hysteresis window, a reduced V_T variation among different L_{ch} accompanied by a decreased I_{on} can be observed with the increased annealing time. Herein, the V_T is defined by the constant current method at which the I_D reaches 1 nA/μm. The extracted V_T as a function of L_{ch} for as-deposited TFTs and O_2-annealed TFTs of different duration is depicted in Fig.7(a). At least 5 devices of the same L_{ch} were measured for the average extraction with error bars standing for the standard deviation. It is found that an overall positively shifted V_T, an alleviated V_T roll-off and a smaller error bar can be achieved with the increased annealing time. On the other hand, the decreased I_{on} can be explained by the increased R_C with annealing time extracted by TLM in Fig.7(b), which is related to the reduction of electron density in the IGZO channel. XPS of O 1s spectrum (Fig.9(b)) shows a significant reduction in oxygen vacancy and hydrogen contamination, indicating the underlying reason for the further improvement.

Figures 8 show the evolution of transfer characteristics of IGZO TFTs of different annealing time with a L_{ch} of 80 nm under gate bias (V_G) of V_T+3 V while the source and drain are grounded for a stress time of 2000 s. The 10 min O_2-annealed TFTs exhibit a remarkably high PBS stability with a small ΔV_T of 53 mV. Interestingly, the ΔV_T is found to transit from negative to positive in Fig. 9(a) with increased annealing time. It is believed that the generation of different types of traps in addition to electron (de)trapping could be the underlying mechanism (Fig.10). The donor-like traps could be the ionized oxygen vacancy and/or hydrogen state [9,10] while the acceptor-like traps may origin from the peroxide state with excessive oxygen [11]. By balancing these two types of traps, a high bias stability could be achieved [12]. Table 1 benchmarks our ALD IGZO TFTs with other recently reported sputtered IGZO TFTs. Our ALD IGZO TFTs show comparable electrical performance with a much thinner T_{ch} and balanced on-state and off-state performance.

Conclusion

In conclusion, we report for the first time ALD IGZO TFTs with extreme scaled T_{ch} of 1.5 nm and L_{ch} of 60 nm, exhibiting outstanding electrical performance including a high I_{on}/I_{off} exceeding 10^{11}, a steep SS of 68 mV/dec, a normal-off operation and a high PBS stability without significant V_T roll-off. This study not only shows that ALD IGZO TFTs with excellent performance and bias stability could be highly promising for BEOL monolithic 3D integration, but also offer some guidance for future oxide semiconductor device optimization.

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Reference: [1] J. Liu et al., IEDM., pp. 21.1-1-21.1.4, 2021. [2] K. Han et al., VLSI, pp. 1-2, 2021. [3] S. Subhechha et al., VLSI, pp. 1-2, 2021. [4] S. Samanta et al., VLSI, pp. 1-2, 2020. [5] C. Wang et al., VLSI, pp. 1-2, 2022. [6] K. Chen et al., VLSI, pp. 1-2, 2022. [7] M. Si et al., Nano Lett, vol.21, p. 500, 2021. [8] P. Liao et al., VLSI, pp. 1-2, 2022. [9] J. Zhang et al., EDL, vol. 44, p. 273, 2023. [10] A. Chasin et al., IEDM., pp. 31.1-1-31.1.4, 2021. [11] S. Choi et al., EDL, vol. 38, p. 580, 2017. [12] D. Zheng et al., IEDM, p. 4.3.1, 2022.

First demonstration of ALD-derived IGZO TFTs with L_{ch} down to 60 nm and T_{ch} down to 1.5 nm.

State-of-art electrical performance including I_{on}/I_{off} of 10^{11}, SS of 68 mV/dec, DIBL of 30 mV/V, normal-off operation, and excellent positive bias stability.

A trap model with possible trap origins for solving V_T roll-off issues and improving bias stability performance.

Fig. 1. Key highlights of this work.

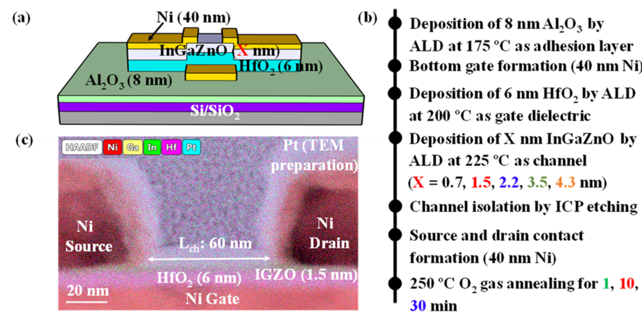

Fig. 2. (a) Device schematic; (c) Fabrication flow of IGZO TFTs; (c) HRTEM of an ultrascaled IGZO TFT with T_{ch} of 1.5 nm and L_{ch} of 60 nm.

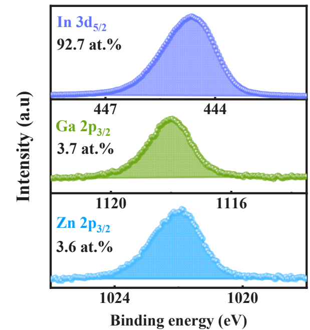

Fig. 3. XPS spectrum of 1.5 nm IGZO suggests an In-rich channel.

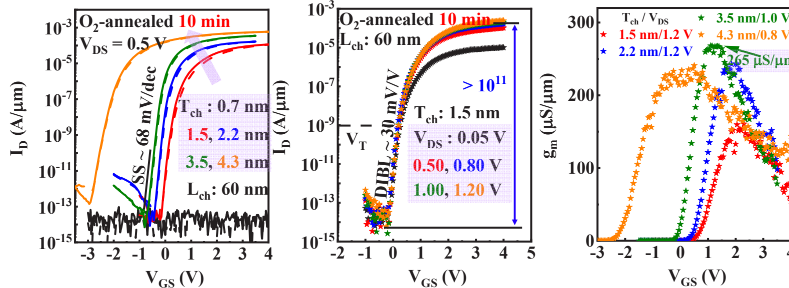

Fig. 4. (a)Transfer curves of IGZO TFTs with L_{ch} of 60 nm and varying T_{ch} under V_{DS} of 0.5 V; (b) Transfer curves of TFTs with T_{ch} of 1.5 nm and L_{ch} of 60 nm under varying V_{DS}; (c) Maximum g_m for TFTs with L_{ch} of 60 nm and varying T_{ch} and V_{DS}.

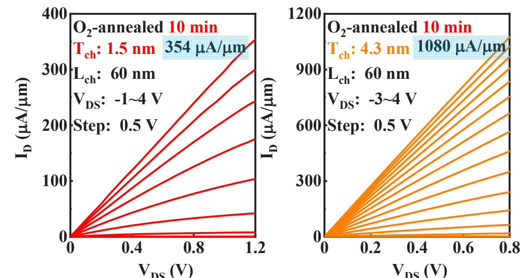

Fig. 5. Output characteristics of IGZO TFTs with L_{ch} of 60 nm and T_{ch} of (a) 1.5 nm, and (b) 4.3 nm, featuring a high I_{on} of 354 μA/μm and 1080 μA/μm, respectively.

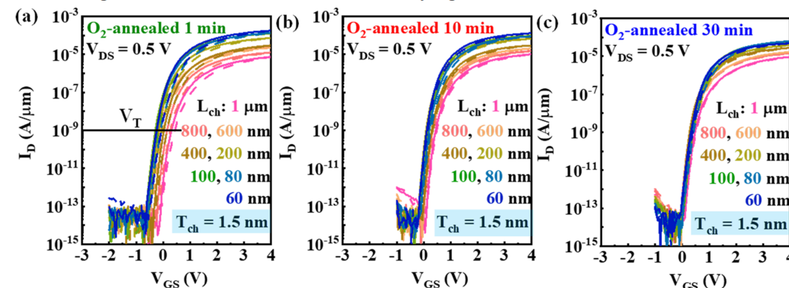

Fig. 6. Transfer characteristics of IGZO TFTs with T_{ch} of 1.5 nm and L_{ch} ranging from 1 μm to 60 nm under V_{DS} of 0.5 V upon (a) 1 min, (b) 10 min, and (c) 30 min O_2 annealing, suggesting a solution to the V_T roll-off issue with a reduced I_{on}.

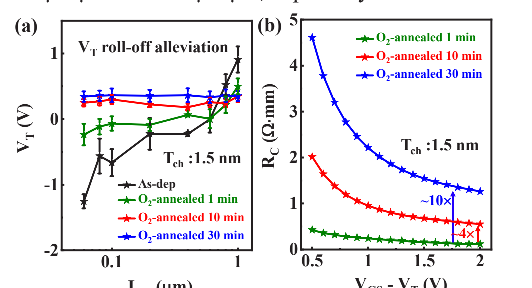

Fig. 7. (a) Extracted V_T as a function of L_{ch}, and (b) R_C as a function of V_{GS}-V_{th} for 1min, 10 min and 30 min O_2-annealed IGZO TFTs with T_{ch} of 1.5 nm.

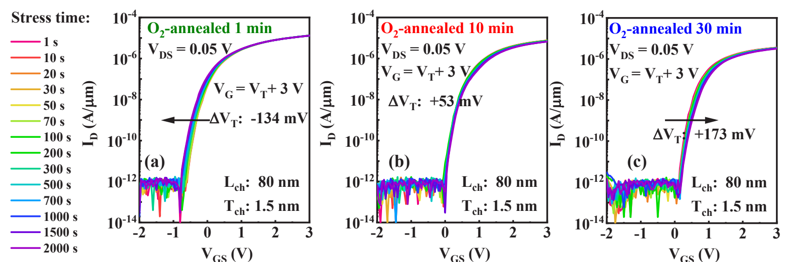

Fig. 8. Evolution of transfer curves of IGZO TFTs with L_{ch} of 80 nm and T_{ch} of 1.5 nm under gate stress voltage of V_T+3 V upon (a) 1 min, (b) 10 min, and (c) 30 min O_2 annealing. The 10 min O_2- annealed TFTs show a high stability to PBS test.

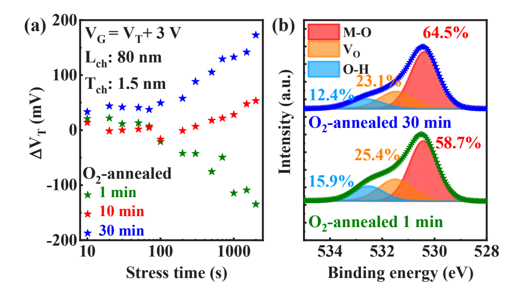

Fig. 9 (a) Extracted ΔV_T as a function of stress time, where a transition from negative to positive can be observed with annealing time (b) O 1s spectrum of 1min and 30 min O_2-annealed IGZO, showing a reduced V_O and OH contamination.

Ref	Structure	T_{ch} (nm)	L_{ch} (nm)	I_{on}/I_{off}	SS (mV/dec)	I_{on} @V_{DS} 1V	DIBL	V_T > 0?
[1]	BG	8	45	10^8	105	55	120	N
[2]	TG	30	100	5×10^8	80	630	45	N
[3]	TG	10	40	10^8	174	NA	NA	N
[4]	BG	3.6	38	2×10^8	87	210	187	N
[5]	BG	8	12.8	2×10^8	NA	635	NA	N
[6]	DG	3	30	5×10^8	63	615	10	Y
This work	BG	**1.5**	**60**	**10^{11}**	**68**	**298**	**30**	**Y**

Table. 1. Benchmarking table for ALD IGZO TFTs with other recently reported sputtered IGZO TFTs. This work presents the first demonstration of ALD scaled IGZO TFTs with desirable electrical performance. V_T stability performance is not evaluated in Ref. [1-6].

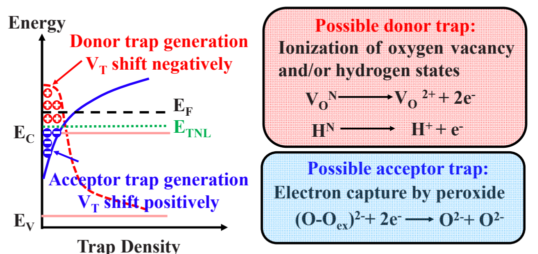

Fig. 10. Models of V_T shifts under PBS test for IGZO TFTs and possible origins of two different types of traps.